A 22–24-GHZ Cryogenically Cooled GaAs FET Amplifier

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Abstract—**This paper describes the design and performance of a cryogenically cooled low-noise FET amplifier operating in the 22–24-GHz range. The amplifier employs five cascaded single-ended gain stages and an integral bandpass filter. Noise temperatures in the 200 K range with an associated gain of 28 dB are typical for the nine cooled units built to date.**

I. Introduction

THE USE OF cryogenic refrigeration to reduce the noise temperature of GaAs FET amplifiers has been shown to be quite beneficial. Noise temperatures close to or below those achievable with parametric amplifiers are believed to be possible [1]. Results have been reported at lower frequencies [2], [3]. This is the first *K*-band amplifier reported that employs cryogenic cooling.

The design relies on an electrical model derived from a physical model of the device. *S*-parameter measurements made at lower microwave frequencies were used to obtain element values for the device model. This model enabled the design of a cascadable amplifier stage with gain over 4 dB and noise figure under 4.6 dB at room temperature.

The design prerequisites include the following:

1) selection of a guiding structure, and
2) device characterization.

The guiding structure selected for the hybrid amplifier and filter circuits is coplanar waveguide. This structure was chosen over microstrip for the following reasons [4], [5].

1) It allows the circuit designer to realize both low- and high-impedance transmission lines without the need for excessively wide or narrow conductor strips.
2) Both series and shunt elements can be realized easily.
3) Parasitic source grounding inductance can be minimized since the need for wraparound grounding ribbons or via holes is eliminated.
4) Coplanar waveguide is less likely to propagate spurious modes than microstrip. This feature, along with the ability to minimize source inductance, enables one to achieve circuits with high reverse isolation (S_{12}). This is essential for a cascadable amplifier stage.

A cross-sectional view of the guiding structure is shown in Fig. 1. The outside conductor strips are electrically grounded. The center strip which is separated from the ground planes by the equal gaps (W) forms the waveguiding structure. The characteristic impedance of a transmission line in this configuration is proportional to the aspect ratio $S/(S+2W)$.

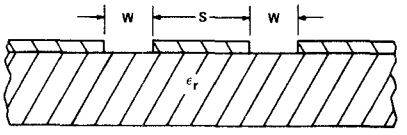

Fig. 1. Coplanar waveguide.

II. Transistor Characterization

Since *K*-band *S*-parameter data was not available for the Mitsubishi MGFC-1403 transistor, *S*-parameter measurements were a critical first step in the design. Direct measurement of *S*-parameters at *K*-band frequencies could not be done because of equipment limitations. Therefore, extrapolation of data measured at lower frequencies was considered.

In order to reliably extrapolate such data, a comprehensive model was created for the transistor. This was done by mounting the FET in a coplanar 50-Ω system and measuring the *S*-parameters of the device. Automatic network analyzer measurements provided reliable, de-embedded device data from 2–15 GHz.

This information was then entered in a computer file containing the circuit model shown in Fig. 2. The program varied several key elements in the file striving to make the circuit analysis match the measured *S*-parameters. After optimization, the model tracked the measured *S*-parameter data quite closely. The model was then analyzed up to 30 GHz, yielding reliable *S*-parameter data for circuit design. To verify the validity of the device model, slotted-line measurements of S_{11} and S_{22} were performed at 22–24 GHz. These measurements agreed quite closely with the predicted S_{11} and S_{22}.

III. Noise Model

After the device model was obtained, it was analyzed to predict the optimum source admittance for the minimum noise figure. This was done by creating a simplified noise model from the device model already obtained. The model is shown in Fig. 3, and the corresponding equations are

$$g_1 = \frac{1}{(Q_1^2+1)R_1} \tag{1}$$

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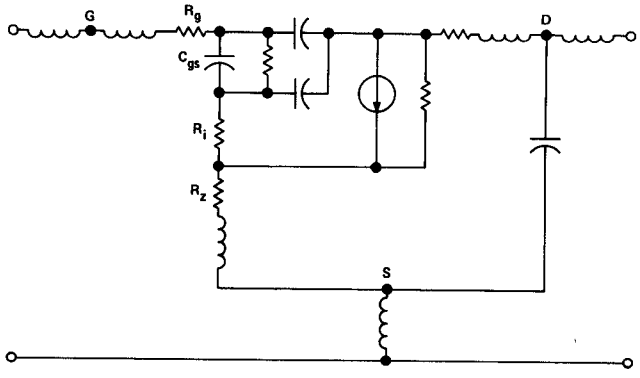


Fig. 2. Transistor model.

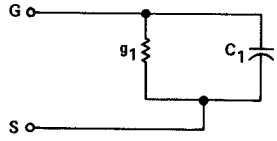


Fig. 3. Noise model.

and

$$C_1 = \frac{Q_1^2 C_{gs}}{(Q_1^2+1)} \tag{2}$$

$$R_1 = R_g + R_i + R_z \tag{3}$$

and

$$Q_1 = \frac{1}{2\pi f c R_1 C_{gs}}. \tag{4}$$

The values R_g, R_i, R_z, and C_{gs}, needed to calculate R_1 and Q_1, are element values obtained from the transistor model shown in Fig. 2. Once values g_1 and C_1 were obtained, the optimum source admittance ($Y_{sopt} = g_{sopt} + jb_{sopt}$) was calculated using (5) and (6)

$$g_{sopt} = g_1\sqrt{1+\frac{1}{A}} \tag{5}$$

$$b_{sopt} = -C_1' = \left(\frac{-Q_1}{Q_1^2+1}\right)\omega C_1. \tag{6}$$

The quantity A is derived from the minimum attainable noise figure (F_{min}) of the device at the frequency of interest through (7)

$$A = \frac{(F_{min}-1)^2}{4F_{min}}. \tag{7}$$

The derivations for (1)–(7) can be found along with a complete description of the noise modeling technique in [6]. The F_{min} at 23 GHz was estimated to be 3.75 dB by extrapolating the manufacturer's data.

IV. Circuit Design

A computer analysis of the circuit in Fig. 2 yielded the device S-parameters shown in Table I. Included in the table is the optimum generator reflection coefficient for the minimum noise figure at 23 GHz. This was found from the noise model already described. Smith Chart techniques were used to design input and output matching networks. Computer optimization was then used to obtain minimum noise figure and flat gain. During a subsequent out-of-band analysis, it was found that a gain peak existed at around 6 GHz. A decoupling network was incorporated in the gate and drain bias circuits to reduce the gain peak. In order to achieve additional rejection at 6 GHz, a bandpass filter module was designed. The filter is cascaded with the amplifier modules in the complete assembly. The final, optimized circuit is shown in Fig. 4 and results of the circuit analysis appear in Table II. The noise-figure analysis at 23 GHz is included in this table.

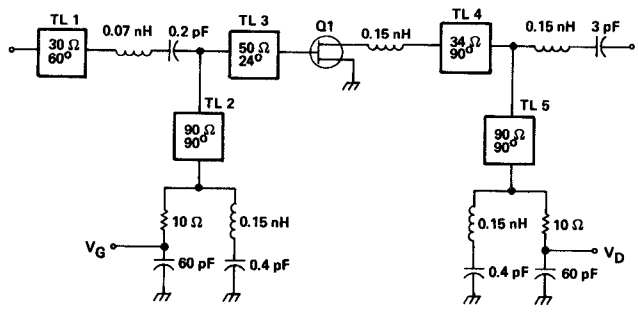


Fig. 4. Amplifier circuit.

TABLE I
Transistor Parameters

Frequency (GHz)	S_{11}	S_{21}	S_{12}	S_{22}	Γ_{opt}
22	0.63/157°	1.15/28.5°	0.137/24°	0.35/-130°	
23	0.64/152°	1.10/24.7°	0.141/25°	0.36/-137°	.63/144°
24	0.65/148°	1.06/21.0°	0.145/26°	0.36/144°	

TABLE II
Amplifier-Circuit Analysis

Frequency (GHz)	S_{11}	S_{21}	S_{12}	S_{22}	S_{21}(dB)	Noise Figure (dB)
22	0.33/86°	1.60/-133°	0.19/-137°	0.19/91°	4.06	--
23	0.23/20°	1.61/-159°	0.21/-160°	0.07/29°	4.13	3.96
24	0.32/-45°	1.51/175°	0.21/180°	014/-85°	3.55	--

V. Construction

The amplifier circuit was built with distributed and lumped elements. The capacitors selected were low-loss parallel plate types. Required inductances were achieved with bond wires or ribbons. Transmission lines and resistors were photoetched on a 0.015-in Au–Cr-deposited alumina substrate. The chrome adhesion layer provided adequate sheet resistance for the thin-film resistors. Fig. 5 is a photograph of an assembled amplifier stage.

Kovar was chosen as the carrier and amplifier housing material because of its excellent thermal stability and close compatibility with alumina over the wide temperature range. Kovar also lends itself to electron-beam welding, which is used to hermetically seal the amplifier.

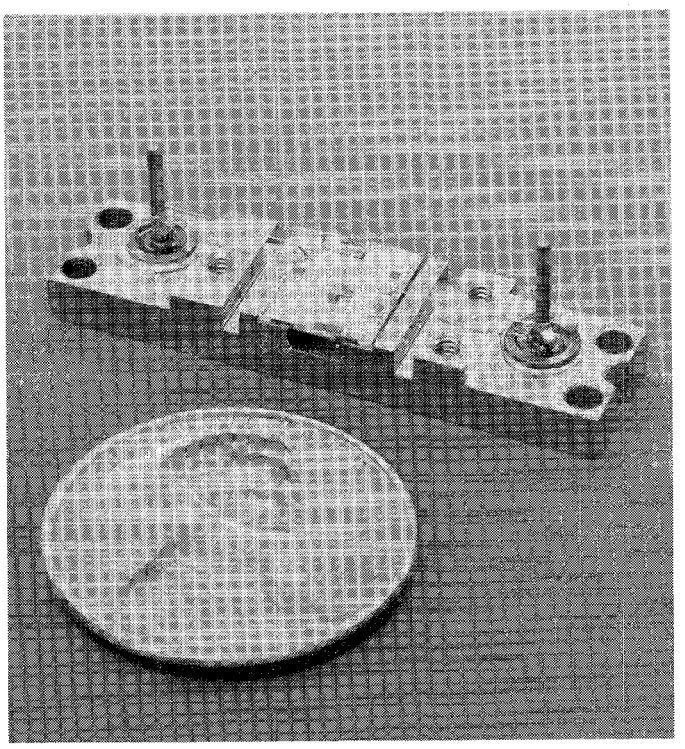


Fig. 5. Assembled amplifier stage.

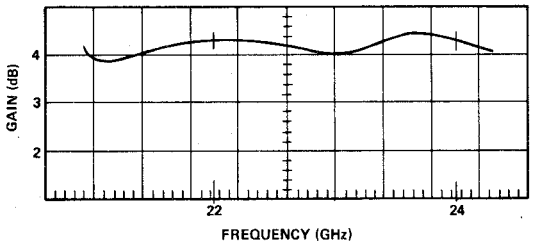


Fig. 6. Measured single-stage gain.

VI. Single-Stage Performance

Gain and return loss were measured using standard swept measurement techniques. The noise figure was measured using an extremely low-noise parametric amplifier as a second stage to minimize measurement uncertainty. The AIL-developed parametric amplifier provided a noise figure of 2.6 and 28 dB of gain at 23 GHz, at 290 K ambient temperature.

Fig. 6 shows the measured gain versus frequency for a typical amplifier stage with corrections for test fixture losses. Connector losses were estimated to be 0.25 dB each at 23 GHz. Fig. 7 shows the measured noise figure of the stage with corrections made for connector loss and second-stage contribution. Figs. 8 and 9 are the measured input and output return losses in the test fixture. Reverse isolation measured was in excess of 17 dB over the 22–24-GHz band.

VII. Cascaded-Amplifier Predicted Performance

The complete amplifier consists of five FET modules cascaded with one bandpass filter module, and a through-line module. The through line is replaced with a sixth gain stage on units intended for room-temperature use only. Fig. 10 shows the block diagram and accompanying gain and noise-temperature budget for the cascaded amplifier. External isolators are placed at the input and output ports of the amplifier, although only the input isolator was included in the noise-temperature budget.

The performance indicated in Fig. 10 is for a single midband frequency. A single-stage unit with a midband gain of 4 dB and noise figure of 4.6 dB at room temperature was assumed for this calculation. The through-line loss

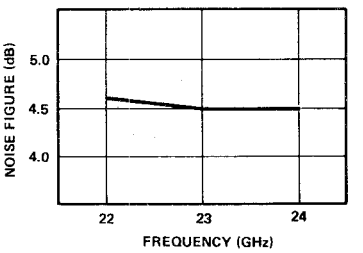


Fig. 7. Single-stage noise figure.

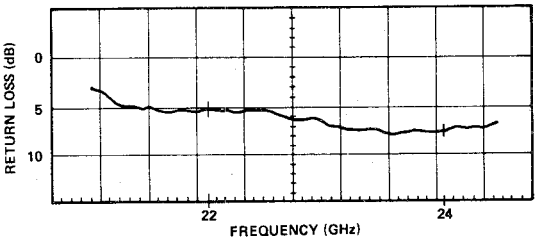


Fig. 8. Single-stage input return loss.

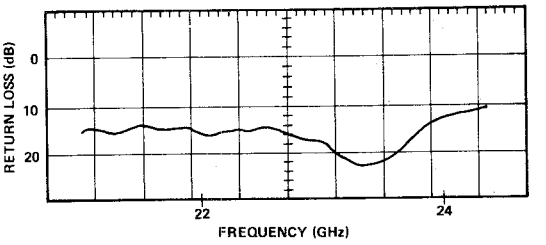
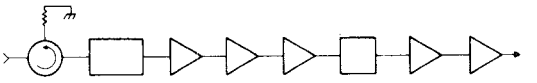


Fig. 9. Single-stage output return loss.



	ISOLATOR	CONNECTOR	STAGE 1	STAGE 2	STAGE 3	BPF AND THROUGH-LINE	STAGE 4	STAGE 5	TOTAL
ROOM TEMP GAIN	0.5 dB	0.25 dB	+4.0 dB	+4.0 dB	+4.0 dB	0.5 dB	+4.0 dB	+4.0 dB	18.75 dB
NET GAIN (ROOM TEMP)	0.89	0.94	2.5	2.5	2.5	0.89	2.5	2.5	72.7 = 18.6 dB
NOISE (K) (ROOM TEMP)	35.8	18.5	546.0	546.0	546.0	35.8	546.0	546.0	
NOISE CONTRIBUTION (ROOM TEMP)	35.8	20.8	652.6	261.0	104.4	2.7	46.9	18.8	1143°
*NET GAIN (77 K)	0.89	0.94	3.54	3.54	3.54	0.89	3.54	3.54	413.9 = 26.2 dB
**NOISE (K) (77 K)	9.5	4.9	109.2	109.2	109.2	9.5	109.2	109.2	
NOISE CONTRIBUTION (77 K)	9.5	5.5	103.5	52.2	20.9	0.7	9.4	3.8	232.5°

*GAIN AT 77 K IS ESTIMATED FROM PAST EXPERIENCE TO BE APPROXIMATELY 1.5 dB HIGHER THEN THE ROOM TEMPERATURE GAIN

**NOISE TEMPERATURE IS ESTIMATED FROM PAST EXPERIENCE TO BE 20% OF THE ROOM TEMPERATURE NOISE TEMPERATURE

Fig. 10. Cascaded gain and noise-temperature prediction.

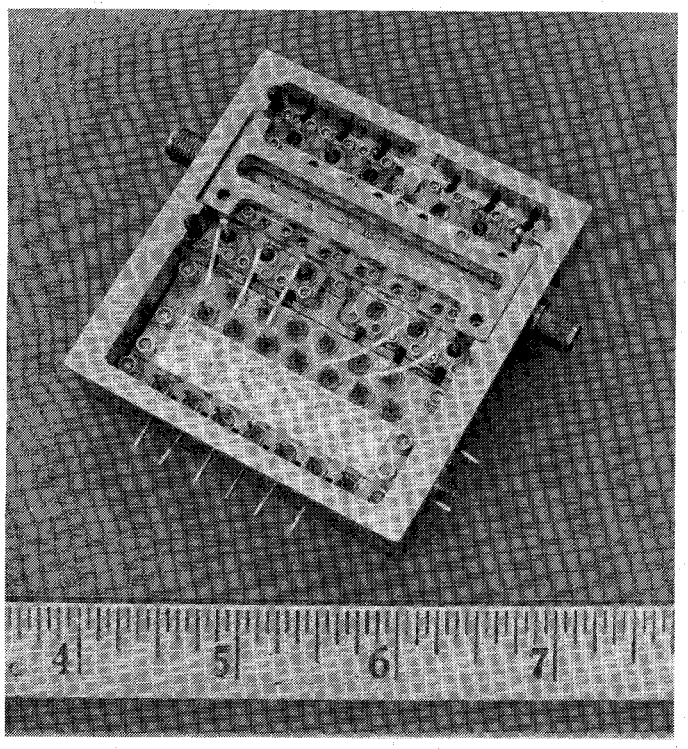


Fig. 11. Integrated amplifier assembly.

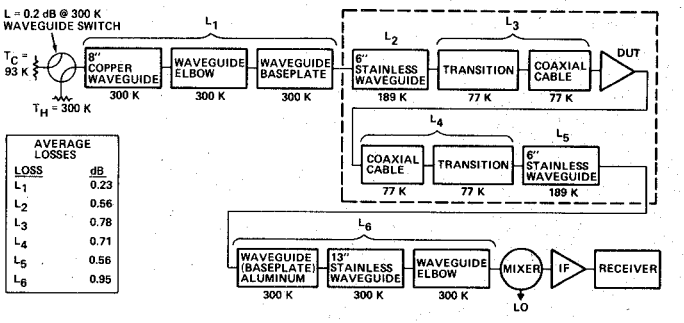


Fig. 12. Cryogenic measurement setup.

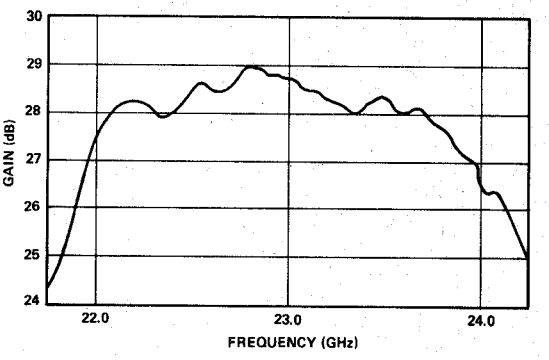


Fig. 13. Amplifier gain at $T_{\text{ambient}} = 77$ K.

was neglected in this estimate. Including isolator loss, the predicted gain is 26.2 dB, and the predicted noise temperature is 232 K for the cryogenically cooled amplifier.

VIII. Integrated Amplifier Construction

The complete amplifier is housed in a Kovar steel chassis as shown in Fig. 11. As it appears in the photograph, the top section contains the cascaded gain and filter stages, located beneath a subcover which provides continuous waveguide walls from input to output. This prevents unwanted spurious responses and enhances reverse isolation. The module occupying the lower section of the chassis is a bias assembly. This circuit provides dc-overvoltage protection, as well as individual device bias adjustment via the terminals along the lower edge of the assembly. The bias terminals located on the same surface as the output connector are for positive and negative supply voltage. The unit features an electron-beam welded top cover for a hermetically sealed package and field-replaceable SMA connectors.

Special consideration was given to the mechanical design because of the extremely low-temperature environment in which the amplifier must operate. Kovar steel was chosen for the housing material as well as for the individual module carriers. The welded-in connector shells which make up the fixed part of the two-piece connectors are also made of Kovar Steel. Kovar is an alloy that is thermally stable and has a temperature coefficient that closely tracks the temperature coefficient of alumina. Tolerancing was kept very close because of the high frequency of operation, but some strain relief was allowed on gold ribbons connecting adjacent stages.

IX. Cryogenic Amplifier Measurements

Gain and noise-temperature measurements were made using a CTI Refrigerator Model No. 1020R. The block diagram in Fig. 12 describes the measurement setup. The area inside the dashed line represents the vacuum vessel which has waveguide input/output ports. Separate slotted-line measurements were made on the sections labeled L_1 through L_6 to determine their individual losses. The diagram shows the physical temperature at which each section was maintained during the cryogenic measurements. The 189 K temperature assigned to L_2 and L_5 is the estimated average temperature of the stainless steel waveguide sections, since they sustained a temperature gradient along their lengths. The reference for the gain measurement was taken outside the vessel (essentially at the input to L_1), and the gain measurement was corrected for the losses listed in Fig. 12. The noise temperature was measured using standard Hot/Cold Y-Factor measurement techniques and corrected for the losses described in Fig. 12.

X. Discussion of Measured Amplifier Performance

Figs. 13 and 14 show the measured gain and noise temperature for a typical unit at an ambient temperature of 77 K. The noise temperature climbs rapidly at the band edges. This is to be expected in a narrow-band design. The increase in gain due to reducing the physical temperature of the unit is seen in Fig. 15. This unit exhibits an average increase of approximately 8-dB gain relative to the room-temperature gain. This is a little better than our 1.5-dB per stage prediction. A room-temperature noise figure is not plotted here, but it was measured. This unit averaged

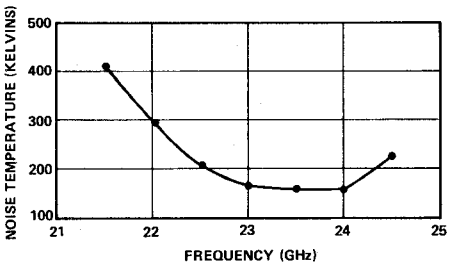


Fig. 14. Amplifier noise temperature at $T_{ambient}$ = 77 K.

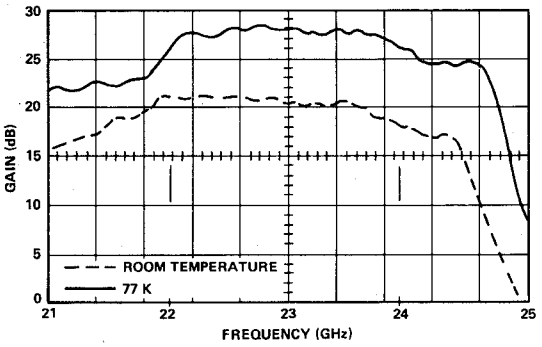


Fig. 15. Amplifier gain versus frequency and temperature.

approximately 5.5 dB, or equivalently 1030 K, at room ambient. This also agrees quite closely with the prediction shown in Fig. 10.

XI. Conclusion

Measured data confirms that *K*-Band GaAs FET amplifiers with noise temperatures approaching those previously achievable only with parametric amplifiers are possible. This performance is a direct result of cryogenically cooling the sealed amplifier. Coplanar waveguide has been shown to be a useful and advantageous circuit medium for use at high microwave frequencies.

It should be noted that this design employs 0.5-μm gate length devices which can no longer be considered state-of-the-art. The new 0.25-μm device technology will undoubtedly result in extremely low-noise temperatures at *K*-band frequencies and higher. It should be noted also that this design exhibits ample performance margin at 77 K ambient for the application for which it was developed. Cooling to lower temperatures (20 K or less) is possible.

Lower temperature cooling, and the use of 0.25-μm FET devices, will probably result in low-noise transistor amplifiers operating at *K*-band with noise temperatures in the 100-K range. At the present, Eaton Corporation AIL Division is investigating these ideas. The AIL Division hopes to publish favorable results in the near future.

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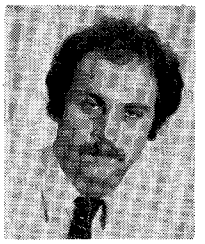

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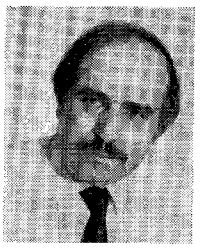

John Pierro (M'78) received the B.E. (E.E.) degree from City College of New York in 1967 and the M.S.E.E. (system science) degree from the Polytechnic Institute of New York in 1978.

He joined the AIL Division of Cutler–Hammer (now Eaton Corporation) in 1967 as an engineer. He presently is a Section Head in the Receiver Systems and Technology Department of the Advanced Technology Systems Division. For the past eight years, he has been responsible for the development of low-noise GaAs FET amplifiers for critical receiver applications. He has authored and coauthored several papers on this work. Previous to this, he was responsible for the design of passive radiometry systems for earth-resources experiments and a variety of analog components, including discriminators and logarithmic amplifiers.